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AN EFFECTIVE DETAILED ROUTING ALGORITHM CONSIDERING ADVANCED TECHNOLOGY NODES*

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Abstract

Detailed routing has become much challenging in modern circuit designs due to the extreme scaling of chip size and the complicated design rules. In this paper, we give an effective algorithm for detailed routing considering advanced technology nodes. First, we present a valid pin-access candidates generation technology for handling complex pin shapes. Then, we propose a tree-based nets components selection algorithm to decide connecting order for multiple nets components. Finally, combined with global routing results and advanced technology nodes, an initial routing results optimization algorithm is presented to achieve the final detailed routing results. Experimental results on industry benchmarks show that, our proposed algorithm not only achieves 100% routability on real industrial cases in a reasonable runtime, but also optimizes total wirelength, total vias and other advanced technology nodes simultaneously.

Keywords detailed routing; advanced technology nodes; pin-access; total vias

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1 Introduction

Routing is considered as the most time-consuming and important stage in the VLSI design flow. In addition, with ever increasing requirements, many new design rules are introduced to satisfy modern industrial demands. Due to the complexity

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of the routing problem, routing is usually divided into two stages: global routing and detailed routing. During the global routing stage, nets are routed on a coarse-grain grid structure with the objective of determining the regions within which each net will be routed. After an approximate routing solution is determined for each net, the detailed routing stage is to find the exact routes of all nets [1]. Since detailed routing is generated based on the global routes, the quality of the final interconnects depends largely on the quality of the global routing solution [27].

Considering advanced technology nodes in detailed routing is a complicated step in the physical design process. A high-performance chip requires that several corresponding metrics need to be evaluated and considered in this dead-or-alive process. With the aim to achieve a better detailed routing result, honoring global routing results can maximize reducing the disturbance to these metrics (e.g., timing, routability [3], manufacturability, skew, and congestion [2, 15, 16]), and so on. Figure 1 is a comparison of routing results of whether or not to take into account the impact of congestion for a net with four pins. If the detailed router routes wires over the region as shown in Figure 1 (a), it will have overlapped wires because of congestion. Figure 1 (b) is a modified detailed routing result considering advanced technology nodes. With the rapid development of modern industrial tools and lithography requirements, satisfying all advanced technology nodes in a detailed routing process is becoming more and more challenging. Therefore, several corresponding metrics need to be managed in different steps during the detailed routing process to meet all constraints in the final detailed routing result.

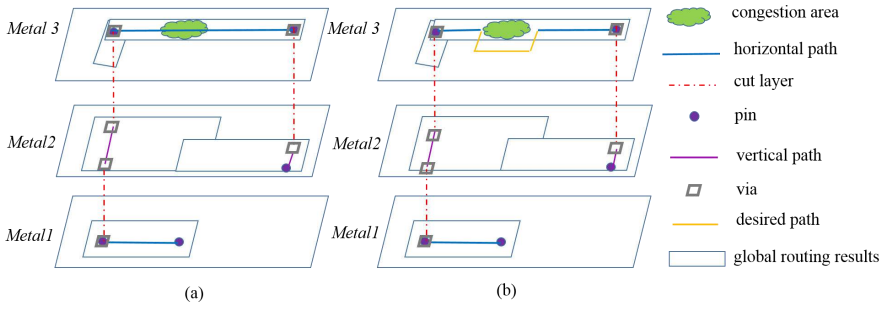

Figure 1: (a) A detailed routing result without considering congestion.
(b) A modified detailed routing result by considering congestion area.

1.1 Previous work

Many works have been presented for VLSI routing based on the shortest path algorithms, which can be divided into two categories: maze routing algorithm and line-search algorithm [4, 5]. The fundamental maze algorithm is *Lee's* algorithm [6],